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Description

Method and System For A Variable Frequency SDRAM Controller

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] Use of SDRAM is nowadays a very popular feature of the system in which large external buffer is necessary. Therefore, the SDRAM controller becomes a fundamental block of the ASIC design for a digital system. A new method to control the SDRAM is presented here, in which a non-regular frequency clock or control signals are involved to best fit timing requirement of a standard SDRAM. As a result, the most efficient timing to access a SDRAM is achieved.

[0003] 2. Description of the Prior Art

[0004] The conventional way to control a SDRAM is using a fix frequency clock as reference, generating all clock-based control signals such as RAS_, CAS_, MA according to this

reference clock (see Figure 1). This is a readily easy and straightforward way to use SDRAM. The fix frequency is constrained and decided by both system bandwidth requirement and working frequency of the logic circuit within an ASIC. To meet some SDRAM's timing parameters given in its specification, the cycle time Tcyc (1/Frequency) is used as the basic unit to generate all control signals. These control signals seen by the SDRAM must be an integer multiple-cycled pulse in unit of Tcyc, since a fix frequency is fed to the SDRAM as a reference clock. Resolution of Tcyc may not be fine enough to generate the best fitting control waveforms to the SDRAM. Therefore, some extra cycle(s) may be accumulated during a read/write access of the SDRAM and it does reduce efficiency of the SDRAM. Figure 2 shows an example that we design timing parameters tRCD= 2*Tcyc, tRP= 2*Tcyc and tRC= 6*Tcyc to meet minimum timing requirement of tRCDmin= 1.4*Tcyc, tPRmin= 1.4*Tcyc and tRCmin=5*Tcyc.

SUMMARY OF THE INVENTION

[0005] The invention provides a method for providing a variable frequency clock for a SDRAM. The method comprises the following steps: (1) receiving a clock with a fixed frequency and a plurality of signals, wherein each the signal

is an interlace combination of a plurality of high level signals and a plurality of low levels signals;(2) extracting a plurality of proper positions from the signals, wherein each low level of each the signal corresponds to a proper position; and (3) amending the frequency of the clock such that each the proper position corresponds to a rising edge of the clock. Herein, each the proper position could located at the center of corresponding the low level; each the proper position could be located at a safety region around the center of corresponding the low level; and each the proper position could be located at a safety region inside corresponding the low level. Further, the step of amending the frequency of the clock is performed by the following steps chosen from the group consisting of the following: multiply frequency, divide frequency, mix the clock with at least one higher frequency clock, using doubled edges of the clock, using and the combination thereof.

[0006] The invention also provides a system for providing a variable frequency clock for a SDRAM. The system comprises the following: (1) a receiver for receiving a clock with a fixed frequency and a plurality of signals, wherein each the signal is an interlace combination of a plurality of high

level signals and a plurality of low levels signals; (2) an extractor for extracting a plurality of proper positions from the signals, wherein each low level of each the signal corresponds to a proper position; and (3) an amender for amending the frequency of the clock such that each the proper position corresponds to a rising edge of the clock. Herein, the extractor could locate each the proper position at the center of corresponding the low level; the extractor could locate each the proper position at a safety region around the center of corresponding the low level; and the extractor also could locate each the proper position at a safety region inside corresponding the low level. Further, the amender is a combination of the parts chosen from the group consisting of the following: frequency multiplier, frequency divider, mixer that receive the clock and at least one higher frequency clock, and the combination thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The foregoing aspects and many of the attendant advantages of the present invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings,

wherein:

[0008] Figure 1. Block Diagram of Regular Frequency Control of SDRAM;

[0009] Figure 2. Examples of Standard SDRAM Timing, A Regular Frequency Clock is Used;

[0010] Figure 3. Block Diagram of Variable Frequency Control of SDRAM; and

[0011] Figure 4. Examples of Revised SDRAM Timing, A Variable Frequency Clock is Used.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] In the following, some preferred embodiments of the invention would be described in greater detail. Nevertheless, it should be recognized that the present invention could be practiced in a wider range in other embodiments beside those explicitly described, and the scope of the present invention is not limited by these expressed embodiments but specified in the accompanying claims.

[0013] One main character of the invention is "Variable Frequency Control of SDRAM. For example, a variable frequency clock source is generated specifically by some elaborate logic circuit (see Figure 3). This circuit is designed so that non-integer multiple-cycled pulse (in unit of Tcyc) can be seen by the SDRAM. The key point of proposed scheme is

to provide higher resolution clock by using either doubled edges of the original clock or higher internal frequency clock as new reference. The newly created clock, along with other control signals, are built-in in ASIC to output best fitting timing to SDRAM. Figure 4 shows an example that we design timing parameters tRCD= 1.5*Tcyc (> tRCDmin=1.4*Tcyc), tRP= 1.5*Tcyc (> tRPmin=1.4*Tcyc) and tRC= 5*Tcyc (≥tRCmin=5*Tcyc) to optimize timing of control signals over SDRAM. Saving of 0.5*Tcyc in tRCD and 0.5*Tcyc in tRP together to make 1*Tcyc saving in tRC.

[0014] The conquered problems and advantages of the invention could be briefly described as the following. The proposed method uses logic circuit to generate variable frequency clock and, according to it, creates related control signals to optimize the access timing toward SDRAM. The variable frequency clocking method removes the limitation on integer-multiple of timing implementation on control signals of SDRAM, thus achieves a more optimized and efficient SDRAM access.

[0015] Of course, it is to be understood that the present invention is not limited by these disclosed embodiments. Various modification and similar changes are still possible

within the spirit of the present invention. In this way, the scope of the present invention should be defined by the appended claims.